In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended): A modularized serial data module for interfacing with a serial data communication interface to an external device operating in accordance with a first serial data protocol that transmits/receives data and also provides power to the modularized serial data module, comprising:

a connector housing for providing a physical interface with the serial data communication interface;

a processor housing disposed adjacent said connector housing and interfacing therewith;

a single chip processor disposed within said processor housing and operable to be powered by the serial data communication interface through said connector housing and also operable to interface with the data portion of the serial data communication interface through said connector housing, said processor operating with a native digital protocol operating in a first time base; and

wherein said single chip processor is operable to provide processing of information based upon data received from the serial data communication interface with the first serial data protocol through said connector housing or processing information with the first serial data protocol for transmission to the serial data communication interface through said connector housing, said [[and]] first serial data protocol different than said native digital protocol and operating on a second time base different from said first time base such that said transmission is asynchronous, wherein said processor receives the serial data generated with the second time base and converts the data to the native protocol with clock recovery; and

said processor having integral therewith a time base referenced to a free running oscillator disposed within said processor housing that requires no external reactive components for the operation thereof, wherein said free running oscillator operates on said first time base which is completely generated one chip with said single-chip processor, which said oscillator provides an operating clock signal to said processor for operation thereof.

2. (Original): The data module of Claim 1, and further comprising a data interface between said processor in said processor housing and external to said processor housing for

transmission of data from the processor exterior to the processor housing or receipt of data generated exterior to said data housing for processing by the said processor.

3. (Original): The data module of Claim 2 wherein said data interface comprises an analog interface.

4. (Original): The data module of Claim 3 wherein said analog interface provides analog output information.

5. (Original): The data module of Claim 3, wherein said analog interface is operable to receive analog data.

6. (Original): The data module of Claim 2, wherein said data interface comprises a digital data interface.

7. (Original): The data module of Claim 6, wherein said digital data interface operates in accordance with a data protocol different than said first serial data protocol.

8. (Original): The data module of Claim 7, wherein said digital data interface operates in accordance with a second serial data protocol different than said first serial data protocol.

9. (Original): The data module of Claim 1 and further comprising a transducer disposed in said processing housing for interfacing between said processor and exterior to said processor housing for receipt of external information generated external to said processor housing or providing of information to the exterior of said processor housing, said transducer interfaced with said processor.

10. (Original): The data module of Claim 9, wherein said transducer is operable to sense exterior information for input to said processor for processing thereof and subsequent transmission to the serial data line through said connector housing.

11. (Original): The data module of Claim 9, wherein said transducer is operable to generate information for output exterior of said processor housing.

12. (Original): The data module of Claim 9, wherein said transducer requires power and the power required thereby is provided through said connector housing and said processor housing.

13. (Original): The data module of Claim 1, wherein the first serial data protocol is a synchronous data protocol.

14. (Original): The data module of Claim 13, wherein the first serial data protocol is associated with a universal serial bus data protocol.

15. (Original): The serial data module of Claim 13, wherein said free running time base utilizes a precision oscillator that does not require a crystal time base.

16. (Currently Amended): A modularized serial data module for interfacing between a first serial data communication interface, operating in accordance with a first serial data protocol, from and to an external device for transmitting and receiving serial data that transmits/receives data and also provides power to the modularized serial data module, and a second serial data communication interface operating in accordance with an associated second serial data protocol that transmits or receives data, comprising:

a connector housing for providing a physical interface with the first serial data communication interface to the external device;

a data interface for providing a physical interface with the second serial data communication interface;

a processor housing disposed adjacent said connector housing and interfacing therewith;

a single chip processor disposed within said processor housing and operable to be powered by the serial data communication interface through said connector housing, and also operable to interface with the data portion of the first serial data communication interface through said connector housing, and to interface with the data portion of the second data communication

interface through said data interface, said processor operating with a native digital protocol operating on a first time base; and

wherein said single chip processor is operable to provide processing of information based upon data received from either the first serial data communication interface in the first serial data protocol through said connector housing or the second serial data communication interface in the second serial data protocol through said data interface, or processing information for transmission to either the serial data communication interface in the first serial data protocol through said connector housing or the second serial data communication interface in the second serial data protocol through said data interface, said first and second serial data protocol different than said native digital protocol and operating on a second time base different from said first time base such that said transmission is asynchronous, wherein said processor receives the serial data generated with the second time base and converts the data to the native protocol with clock recovery.

17. (Original): The data module of Claim 16, wherein said data interface comprises an analog interface.

18. (Original): The data module of Claim 17, wherein said analog interface provides analog output information.

19. (Original): The data module of Claim 18, wherein said analog interface is operable to receive analog data.

20. (Original): The data module of Claim 16, wherein said data interface comprises a digital data interface.

21. (Previously Presented): The data module of Claim 20, wherein said digital data interface operates in accordance with said second data protocol different than said first serial data protocol.

22. (Cancelled)

23. (Original): The data module of Claim 16, wherein the first serial data protocol is a synchronous data protocol.

24. (Original): The data module of Claim 23, wherein the first serial data protocol is associated with a universal serial bus data protocol.

25. (Previously Presented): The serial data module of Claim 24, wherein said processor utilizes a free running time base generated within said connector housing.

30. (Previously Presented): The serial data module of Claim 24, wherein said processor utilizes a free running time base that utilizes a precision oscillator that does not require a crystal time base.